

Event Report

Project Competition on ‘VLSI Design ‘based on FPGA Board

- ❖ Date of conduction: **16 April’2015 and Time of conduction : 10:00 AM - 01:30 PM**
- ❖ Venue: A316 (ME, Communication System Laboratory)
- ❖ Name of the Faculty Coordinator’s for the event
 - **Prof. Deepak Parashar**
 - **Prof. Mayank Mahant**
- ❖ Number of students participated: **56 (UG, EC third Year Students)**
- ❖ The event is supported by **ISTE student chapter**

The department of E&C has organized an event under ISTE student chapter titled “Project Competition on ‘VLSI Design ‘based on FPGA Board” as a part of their core subject “VLSI Design and Technology” for the UG Third Year, Electronics and Communication students Organized by Department of Electronics & Communication at G. H. Patel College of Engineering & Technology, Vallabh Vidyanagar, Gujarat on 16th April’2015

The students have demonstrated projects on various topics related to VLSI domain and implemented on FPGA Board. The students have presented their innovative ideas through projects in the group of three. The above stated faculty and some other faculty members have encouraged and help them to take the benefit of the event in a way to understand the importance of VLSI Domain.

Few topics are as per following:

- 8 bit Multiplier
- Adder/ Subtractor
- Finite state machines
- Counter based projects
- Edge detector
- Digital clock etc.....

The undersigned faculty members are the organizer of the event.

Prof. Deepak Parashar,
Prof . Mayank Mahant

The undersigned were the jury faculty member for the event.

Dr. Bhaskar Thakkar (Head of the EC Dept.)

Event Notice



G H PATEL COLLEGE OF ENGINEERING & TECHNOLOGY
DEPARTMENT OF ELECTRONICS & COMMUNICATION

MINI PROJECT DEMONSTRATION/COMPETITION ON **'VLSI DESIGN'**

We are going to organize one day Mini Project competition under ISTE student chapter for the third year BE (Electronics and Communication) students of EC department on Thursday 16th april, 2015.

The schedule for the same is as mentioned below:

Time: 10:00 AM - 01.30 PM

Date: 16th April, 2015.

Venue: A-316

Prof. Deepak Parashar and
Prof. Mayank Mahant
Faculty Coordinator's

Dr. B. V. Thakkar
(Prof. & Head)
EC Department

❖ The event is supported by ISTE student chapter

16th April, 2015

To,

Prof. Vijay Makwana,

Faculty Advisor,

GCET ISTE Students Chapter

Sub.:- Financial support for organizing a Mini Project Competition on VLSI Design event by EC students

Dear Sir,

EC department in association with GCET ISTE student's is going to organize one day Mini Project competition under ISTE student chapter for the third year BE (Electronics and Communication) students of EC department on Thursday 16th april, 2015.

The schedule for the same is as mentioned below:

Time: 10:00 AM - 01.30 PM, Date: 16th April, 2015.

Venue: A-316

In order to encourage the students, we would like to present 1st prize and 2nd prize to them.

We request you to kindly provide necessary financial support of approximately Rs. 300/- for organizing the event.

Thanking you.

Prof. Deepak Parashar

(Event Coordinator)

Students Attendance sheet

Date: 16/04/2015

Attendance Sheet

MINI PROJECT DEMONSTRATION/COMPETITION ON 'VLSI DESIGN'

Sr. No	EN. NO.	NAME OF THE STUDENT'S	TITLE OF THE PROJECT	SIGN
②	120110111001	Patel Parth	BCD TO SEVEN SEGMENT CODE CONVERT	Patel Parth
	120110111003	Patel Ankit		
	120110111002	Patel Rusht		
	120110111019	Dave Ankit		
5	120110111014	Patel Anil	digital clock in VHDL	Anil Patel
6	120110111017	Abhishek bhunushali		
7	120110111005	shivani Patel		
8	120110111007	Asmita mehta		
✓	120110111012	Rahul Patel	Multiplier	Rahul Patel
	120110111029	Smit kothari		
	120110111049	Reema Zala		
	120110111018	Vaishali Patil		
13	120110111045	Roshan Chisty	PRIORITY ENCODER.	Roshan Chisty
14	120110111048	Vinod Mehta		
15	120110111051	Bhadrak Panchal		
16	120110111054	Nikhil Varma		
17	120110111034	vaishali daiya	Finite state machine.	Vaishali Daiya
18	120110111026	Bhavsa Kishan		
19	120110111027	Amiav Vakharia		
20	120110111016	Hansh Anilsharma		
21	220114111001	Raj Shah	2's complement	Raj Shah
22	120110111058	Deep Patel		
23	120110111061	Shubham Tripathi		

(Deepak Parashar)

Date: 16/04/2015

Attendance Sheet

MINI PROJECT DEMONSTRATION/COMPETITION ON 'VLSI DESIGN'

Sr. No	EN. NO.	NAME OF THE STUDENT'S	TITLE OF THE PROJECT	SIGN
	13011311011	Deep Shek	Universal Shift Counter 99.	[Signatures]
	13011311004	Kartikay Jashi		
	12011011059	Nikhil Chodhary		
	12011011011	Hanshil Joshi	Half subtractor	[Signatures]
	12011011021	Daloo Patel		
	12011011030	Dhruv Vyas		
	13011311043	Vahana Yama	Parallel to serial converter	[Signatures]
	12011311002	Patel Dipak		
	13011311010	Ruti Rabadi	Traffic Light Controller	[Signatures]
	13011311009	Rina Patel		
	13011311002	Prayansh M Daware	Serial-Parallel Converter	[Signatures]
	13011311003	Shubham Jethawa		
	13011311001	Jolly chudasama	Edge detector	[Signatures]
	12011411002	Rashmi Pujari		
	12011031037	Patel Ashwini R.	Johnson Counter	[Signatures]
	13011311007	Bhavin Patel		
	12011011023	Jaydeep Shah		
	12011011028	Tilak Patel		
	12011011031	Sanya Engineer		
	12011011005	Sangni Vidhi	Ring Counter	[Signatures]
	12011011006	Paridya Vidhi		
	12011011010	Katgami		
	12011011013	Nalini Shumya		

Deepak

(Deepak Parashar)

Date: 16/04/2015

Attendance Sheet

MINI PROJECT DEMONSTRATION/COMPETITION ON 'VLSI DESIGN'

SR. No	EN. NO.	NAME OF THE STUDENT'S	TITLE OF THE PROJECT	SIGN
1.	20110111056 60 44	Jessica Desai Radhika Patel Astha Desai	Full Subtractor	Jessica Desai Radhika Patel Astha Desai
	120110111033 120110111038 120110111041	Bhavini majethia nidhi Mahambhatt Ankita mistry	Edge detector	Bhavini majethia nidhi Mahambhatt Ankita mistry
	130113111005 130113111006 120110111077	Kamdevale Anand Kamling Anand Prasanna Oza	Digital clock	Kamdevale Anand Kamling Anand Prasanna Oza
	120110111022 35 43	Kainab Rawat Gaurav Balani Dhanvi Faldar	Binary down Counter	Kainab Rawat Gaurav Balani Dhanvi Faldar
	120110111053 49 52	Shivangi Patel Jijal Patel Shriya Khora	ALU using case condition	Shivangi Patel Jijal Patel Shriya Khora

(Deepak Patil
Deepak Patil)

Event Feedback given by students

Dept. of Electronics & Communication Engrg., GCET
EVENT FEEDBACK FORM

Name of an Event: VLSI Project Date of an Event: 16/4/15
Course associated with an Event: VLSI

Sl. No.	FEEDBACK	CHOICE
1	Do you think the event has increased your interest in additional learning?	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
2	Do you think the event has improved practical knowledge of Electronics & Communication Engineering?	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
3	Do you think the event has helped you to realize yourself as a team member?	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
4	Do you think the event has provided you a platform to learn something beyond the syllabus of a course/contents in the curriculum?	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
5	Do you think the event has helped you in improving your communication skill in representing your technical ideas?	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO

Suggestions: _____

Signatures with Enrolment No.s:
Amith 12011011041
Abhishek 12011011036

Dept. of Electronics & Communication Engrg., GCET
EVENT FEEDBACK FORM

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Course associated with an Event: VLSI

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Suggestions: _____

Signatures with Enrolment No.s:
Saravali 12011011022
Gunwar 12011011043
Salad 12011011035

Dept. of Electronics & Communication Engrg., GCET
EVENT FEEDBACK FORM

Name of an Event: VLSI PROJECT Date of an Event: 16/4/15
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5	Do you think the event has helped you in improving your communication skill in representing your technical ideas?	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO

Suggestions: _____

Signatures with Enrolment No.s:
12011011033
12011011048
12011011045
12011011051
12011011054

Dept. of Electronics & Communication Engg., GCET

EVENT FEEDBACK FORM

Name of an Event:

Date of an Event: 16/4/15

Course associated with an Event: VLSI

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4	Do you think the event has provided you a platform to learn something beyond the syllabus of a course contents of the current semester?	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
5	Do you think the event has helped you to improve your communication skill for representing your technical ideas?	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO

Suggestions

Signature/s with Enrollment No.:

120110111005 [Signature]
006 [Signature]
010 [Signature]
013 [Signature]

Dept. of Electronics & Communication Engg., GCET

EVENT FEEDBACK FORM

Name of an Event:

Date of an Event: 16/4/15

Course associated with an Event: VLSI

Sr. No.	FEEDBACK	CHOICE
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5	Do you think the event has helped you to improve your communication skill for representing your technical ideas?	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO

Suggestions

Signature/s with Enrollment No.:

Traffic light control
1301k3111010 [Signature]
130113111009 [Signature]

16/4/15

VLSI Dept. of Electronics & Communication Engg., GCET

EVENT FEEDBACK FORM

Name of an Event: ALU

Course associated with an Event:

120110111053 [Signature]
120110111049 [Signature]
120110111052 [Signature]

Sr. No.	FEEDBACK	CHOICE
1	Do you think the event has increased your interest in additional learning?	<input checked="" type="checkbox"/> YES <input type="checkbox"/> NO
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Suggestions

Signature/s with Enrollment No.:

Students Certificate's



 

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
G. H. PATEL COLLEGE OF ENGINEERING AND TECHNOLOGY, V.V.NAGAR

CERTIFICATE OF PARTICIPATION

This certificate is awarded 'second position' to PATEL RUSHI N. for his / her participation in one day Mini Project Competition on 'VLSI Design 'based on FPGA Board' under ISTE student chapter for the 3rd Year Electronics and Communication undergraduate students on 16/04/2015, by Department of Electronics & Communication at G. H. Patel College of Engineering & Technology, Vallabh Vidyanagar, Gujarat.


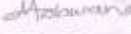


 Prof. Deepak Parashar Event Coordinator	 Dr. Vijay Makwana ISTE Coordinator	 Dr. B V Thakkar Head of EC Department	 Dr. Himanshu Soni Principal, GCET
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
G. H. PATEL COLLEGE OF ENGINEERING AND TECHNOLOGY, V.V.NAGAR

CERTIFICATE OF PARTICIPATION

This certificate is awarded 'first position' to PATEL ASHISH R. for his / her participation in one day Mini Project Competition on 'VLSI Design 'based on FPGA Board' under ISTE student chapter for the 3rd Year Electronics and Communication undergraduate students on 16/04/2015, by Department of Electronics & Communication at G. H. Patel College of Engineering & Technology, Vallabh Vidyanagar, Gujarat.

 Prof. Deepak Parashar Event Coordinator	 Dr. Vijay Makwana ISTE Coordinator	 Dr. B V Thakkar Head of EC Department	 Dr. Himanshu Soni Principal, GCET
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Event Photographs



