Event Report

Project Competition on 'VLSI Design 'based on FPGA Board

- ◆ Date of conduction: 16 April'2015 and Time of conduction : 10:00 AM 01:30 PM
- Venue: A316 (ME, Communication System Laboratory)
- ✤ Name of the Faculty Coordinator's for the event
 - Prof. Deepak Parashar
 - Prof. Mayank Mahant
- Number of students participated: **56 (UG, EC third Year Students**)
- The event is supported by ISTE student chapter

The department of E&C has organized an event under <u>ISTE student chapter</u> titled "Project Competition on 'VLSI Design 'based on FPGA Board" as a part of their core subject "<u>VLSI Design and Technology</u>" for the UG Third Year, Electronics and Communication students Organized by Department of Electronics & Communication at G. H. Patel College of Engineering & Technology, Vallabh Vidyanagar, Gujarat on 16thApril'2015

The students have demonstrated projects on various topics related to VLSI domain and implemented on FPGA Board. The students have presented their innovative ideas through projects in the group of three. The above stated faculty and some other faculty members have encouraged and help them to take the benefit of the event in a way to understand the importance of VLSI Domain.

Few topics are as per following:

- 8 bit Multiplier
- Adder/ Subtractor
- Finite state machines
- Counter based projects
- Edge detector
- Digital clock etc.....

The undersigned faculty members are the organizer of the event.

Prof. Deepak Parashar, Prof . Mayank Mahant

The undersigned were the jury faculty member for the event.

Dr. Bhaskar Thakkar (Head of the EC Dept.)

Event Notice





G H PATEL COLLEGE OF ENGINEERING & TECHNOLOGY

DEPARTMENT OF ELECTRONICS & COMMUNICATION

MINI PROJECT DEMONSTRATION/COMPETITION ON <u>'VLSI Design'</u>

We are going to organize one day Mini Project competition under ISTE student chapter for the third year BE (Electronics and Communication) students of EC department on Thursday 16th april, 2015.

The schedule for the same is as mentioned below:

Time: 10:00 AM - 01.30 PM

Date: 16th April, 2015.

Venue: A-316

Prof. Deepak Parashar and Prof. Mayank Mahant Faculty Coordinator's Dr. B. V. Thakkar (Prof. & Head) EC Department

✤ The event is supported by ISTE student chapter

16th April, 2015 To, Prof. Vijay Makwana, Faculty Advisor, GCET ISTE Students Chapter

Sub.:- Financial support for organizing a Mini Project Competition on VLSI Design event by EC students

Dear Sir,

EC department in association with GCET ISTE student's is going to organize one day Mini Project competition under <u>ISTE student chapter</u> for the third year BE (Electronics and Communication) students of EC department on Thursday 16th april, 2015.

The schedule for the same is as mentioned below:

Time: 10:00 AM - 01.30 PM, Date: 16th April, 2015.

Venue: A-316

In order to encourage the students, we would like to present 1st prize and 2nd prize to them.

We request you to kindly provide necessary financial support of approximately Rs. 300/- for organizing the event.

Thanking you.

Prof. Deepak Parashar (Event Coordinator)

Students Attendance sheet

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Date: 16/04/2015

Attendance Sheet

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Date: 16/04/2015

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Event Feedback given by students

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Students Certificate's

GCET DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING G. H. PATEL COLLEGE OF ENGINEERING AND TECHNOLOGY, V.V.NAGAR CERTIFICATE OF PARTICIPATION This certificate is awarded 'second position' to PATEL RUSHI for his / N her participation in one day Mini Project Competition on 'VESI Design 'based on FPGA Board" under ISTE student chapter for the 3rd Year Electronics and Communication undergraduate students on 16/04/2015, by Department of Electronics & Communication at G. H. Patel College of Engineering & Technology, Vallabh Vidyanagar, Gujarat. Dr. Himfathu Sont Herrans 3° Prof. Deeph Parashar Dr. Vijay Malewana Dr. B V Thakliar Event Condinator ISTE Coordinator Head of EC Department Principal. GCET GCET DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING G. H. PATEL COLLEGE OF ENGINEERING AND TECHNOLOGY, V.V.NAGAR FICATE (This certificate is awarded 'first position' to PATEL ASHISH R. for his / her participation in one day Mini Project Competition on "VLSI Design "based on PPGA Board" under ISTE student chapter for the 31d Year Electronics and Communication undergraduate students on 16/04/2015, by Department of Electronics of Communication at G. H. Patel College of Engineering & Technology, Vallabh Vidyanagar, Gujarat. Oh: CB -Aspenana Dr. Himanshu Soni Prof. Deepar Parashar Dr. B V Thakkar Dr. Vijay Makwana * Head of EC Department Principal, GCET ISTE Coordinator Event Coordinator

Event Photographs





